KAF - 0400C

768(H) x 512(V) Pixel

Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Microelectronics Technology Division

Rochester, New York 14650

Revision 0

August 2, 1993

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-2010
Phone (716)-722-4385 Fax (716)-477-4947

TABLE OF CONTENTS

FIGURES

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

1.1 Features

- **Front Illuminated Full-Frame Architecture**
- **768(H) x 512(V) Photosensitive Color Pixels**
- **9μm(H) x 9μm(V) Pixel Size**
- **6.91mm(H) x 4.6mm(V) Photosensitive Area**
- **8.4mm(H) x 5.5mm(V) Chip Size**
- **3:2 Aspect Ratio**
- **70% Fill Factor**
- **Single Readout Register**
- **Proprietary 2 phase Buried Channel Processing**
- **Additional On-Chip Dark Reference Pixels**
- **Low Dark Current (<10pA/cm^2 @ T=25^{o}C)**
- **High Dynamic Range (>71 dB)**
- **High Output Sensitivity (10μV/e$^-$)**
- **Data Rates up to 20MHz**
- **No Image Lag**

1.2 Description

The KAF-0400C is a high performance silicon charge-coupled device (CCD) designed for a wide range of color image sensing applications in the 0.4μm to 1.1μm wavelength band. Common applications include scientific, military, machine and industrial vision, copystand, film digitizers and electronic still photography among others. The device is readily available in three defect grades including a cosmetically perfect grade (Class 0) even at room temperature.

The device is built with an advanced true two-phase, two-polysilicon, NMOS CCD technology. This technology aids in the reliable fabrication of small pixel sizes. It also contributes to a higher short-free yield and aids in lowering the dark current without compromising charge capacity. The extremely low dark current of the KAF-0400C makes this device suitable for low light imaging applications. CCD cooling requirements, which is employed in the most demanding systems, can be significantly reduced using this device. The on-chip output amplifiers have been specially designed to perform at a high speed operation (45MHz BW) at low noise levels (15e$^-$ rms) to increase frame rate.

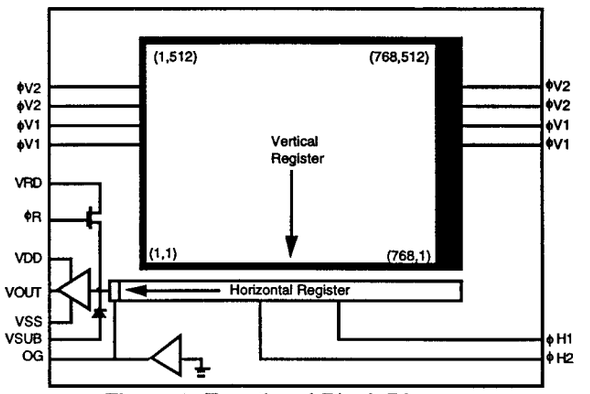


Figure 1 Functional Block Diagram

Shaded areas represent 4 non-imaging pixels at the beginning and 12 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

1.3 Architecture

Refer to the block diagram above. The KAF-0400C consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and one output amplifier. Both registers incorporate two level polysilicon and true two-phase buried channel technology. The vertical register consists of 9μm x 9μm photocapacitor sensing elements (pixels) which also serves as the transport mechanism. The pixels are arranged in a 768(H) x 512(V) array in which an additional 16 columns and eight rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. Because there is no storage array, this device must be synchronized with strobe illumination or shuttered during readout. Pixel 'binning' is possible in both the horizontal and vertical direction thus increasing sensitivity at the expense of resolution.

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

1.4 Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (ϕV1, ϕV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will spill into the lateral overflow drain (LOD) and drain off-chip thus isolating adjacent pixels from excess signal. This is referred to as antiblooming control.

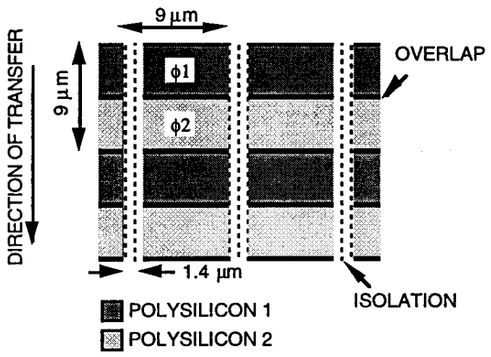


Figure 2 Pixel Drawing - Top View

1.5 Charge Transport

Integrated charge is transported to the output in a two step process. Columns of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagram, integration of charge is performed with ϕV1 and ϕV2 held low. Transfer to horizontal CCD begins when ϕV1 is brought high causing charge from the ϕV1 and ϕV2 gates to combine under the ϕV1 gate. ϕV1 and ϕV2 now reverse their polarity causing the charge packets to 'spill' forward under the ϕV2 gate of the next pixel. The rising edge of ϕV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the ϕV1 electrode of the next pixel. The sequence completes when ϕV1 is brought low while the horizontal CCD reads out the first line of charge using traditional complementary clocking (using ϕH1 and ϕH2 pins) as shown. Clocking of the vertical register in this way is known as accumulation mode clocking. The falling edge of ϕH2 forces a charge packet over the output gate (OG) onto the output node (floating diffusion) and sensed off-chip. The cycle repeats until all lines are read.

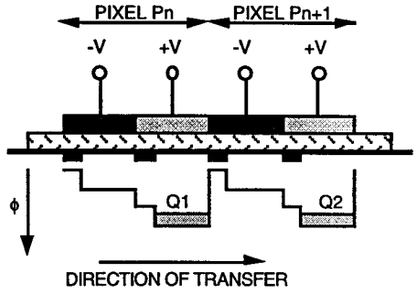


Figure 3 True 2 Phase CCD Cross Section

1.6 Output Structure

Charge packets received from the horizontal register are dumped onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression $\Delta V_{fd}=\Delta Q/C_{fd}$. A two stage source-follower amplifier is used to buffer this voltage change to the outside world. The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the charge has been sensed off-chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

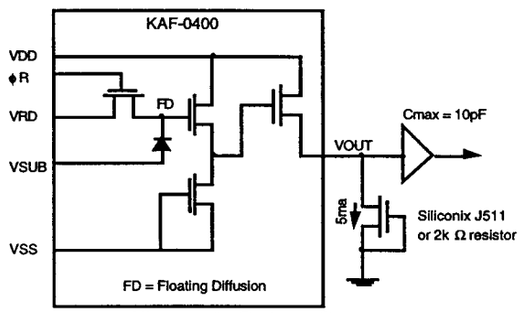
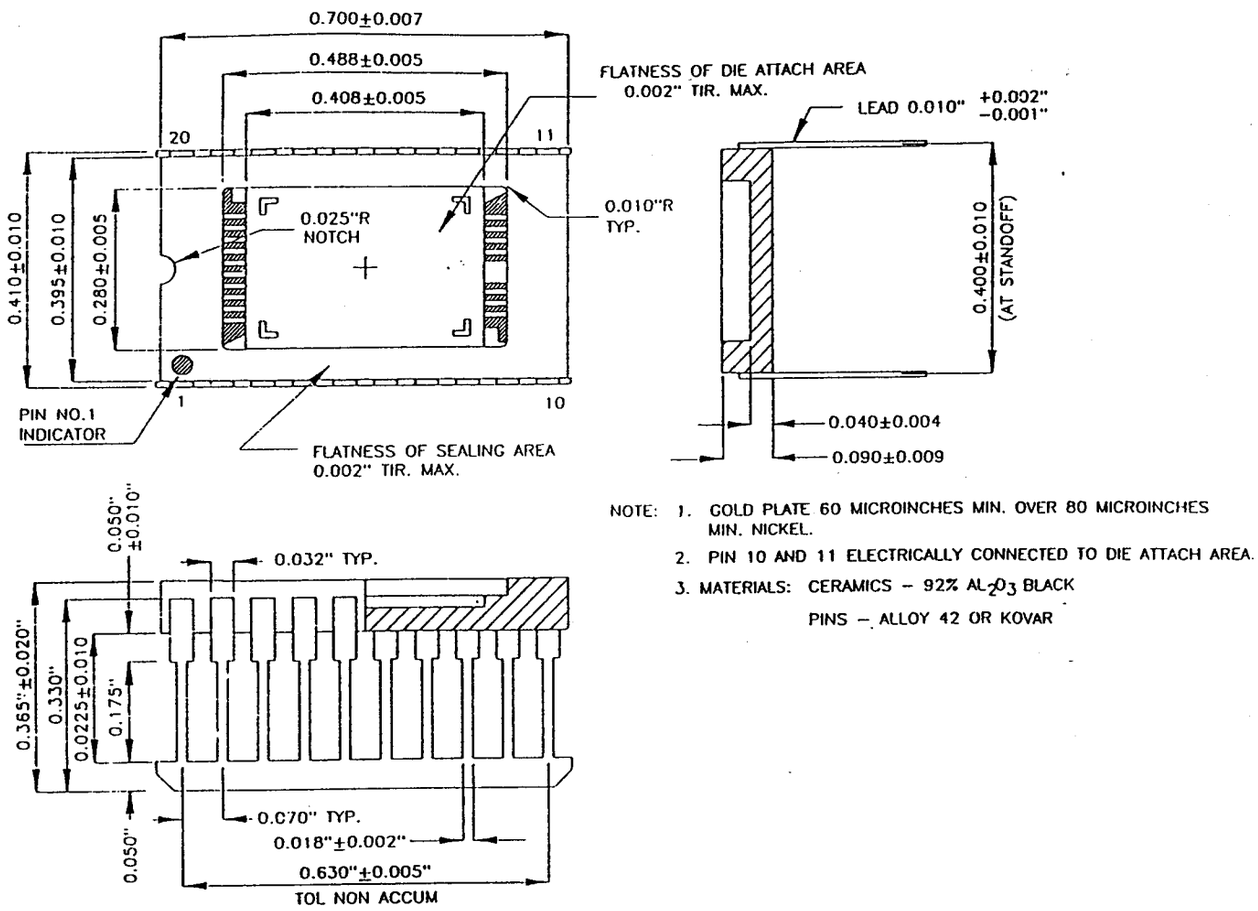


Figure 4 Output Structure

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

1.7 Package Configuration



NOTE:
1. GOLD PLATE 60 MICROINCHES MIN. OVER 80 MICROINCHES MIN. NICKEL.
2. PIN 10 AND 11 ELECTRICALLY CONNECTED TO DIE ATTACH AREA.
3. MATERIALS: CERAMICS – 92% AL_2O_3 BLACK
   PINS – ALLOY 42 OR KOVAR

Figure 5 Packaging Diagram

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

2.1 Pin Description

PIN #	SYMBOL	DESCRIPTION	NOTES
12, 13, 18, 19	V1	Vertical (Parallel) CCD Clock - Phase 1	1
14, 15, 16, 17	V2	Vertical (Parallel) CCD Clock - Phase 2	2
10, 11	VSUB	Substrate	
1	OG	Output Gate	
5	ϕR	Reset Clock	
4	VRD	Reset Drain	
6	VSS	Output Amplifier Return	
2	VOUT	Video Output	
3	VDD	Output Amplifier Supply	
7	ϕH1	Horizontal (Serial) CCD Clock - Phase 1	
8	ϕH2	Horizontal (Serial) CCD Clock - Phase 2	
20	GUARD	Guard Ring	

Notes: 1 - Pins 12, 13, 18, 19 must be connected together - only one Phase 1 clock driver is required
2 - Pins 14, 15, 16, 17 must be connected together - only one Phase 2 clock driver is required

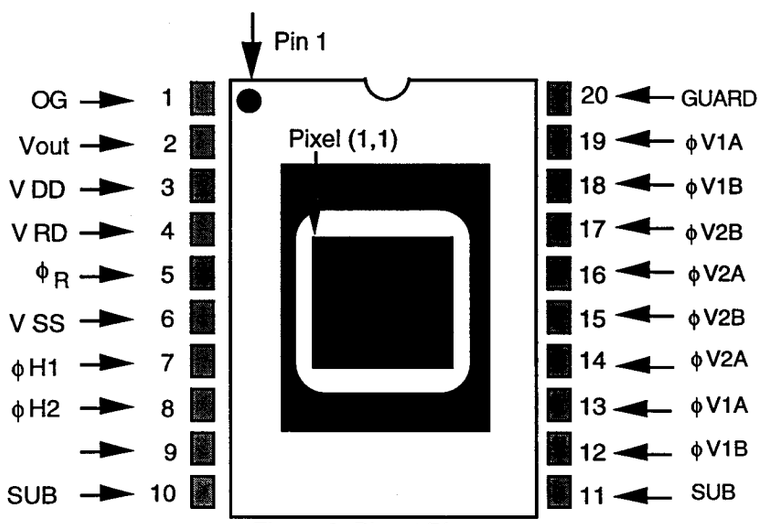


Figure 6 Pinout Diagram

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

2.2 Absolute Maximum Ratings

		Minimum	Maximum	Unit	Conditions
Temperature	Storage	-100	+80	C	At Device
	Operating	-50	+80		
Voltage	All Clocks	-10	+10	V	VSUB = OV
	OG	-1	+6		
	VRD, VSS, VDD, GUARD	-0.5	+16		
Current	Output Bias Current (IDD)		10	mA	
Capacitance	Output Load Capacitance (CLOAD)		10	pF	
Frequency/Time	ϕV1, ϕV2 Pulse Width	4		µs	
	ϕH1, ϕH2		20	MHz	
	ϕR Pulse Width	10		ns	

Warning: For maximum performance, built-in gate protection has been added only to the OG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage. Consult Eastman Kodak for proper handling procedures.

2.3 DC Operating Conditions

		Minimum	Nominal	Maximum	Unit	Pin Impedance
VSUB	Substrate	0.0	0.0	0.0	V	Common
VDD	Output Amplifier Supply	+14.75	+15.00	+15.25	V	5pf, 2kΩ
VSS	Output Amplifier Return	0.6	0.7	1.5	V	5pf, 2kΩ
VRD	Reset Drain	+9.75	+10.00	+10.25	V	5pf, 1MΩ
OG	Output Gate	1	3	5	V	5pf, 10MΩ
GUARD	Guard Ring, LOD	+5.0	+7.0	+10	V	350pF, 10MΩ

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

2.4 AC Clock Level Conditions

			Minimum	Nominal	Maximum	Unit	Pin Impedance
ϕV1	Vertical Clock - Phase 1	Low	-8.5	-8.0	-7.5	V	10nF, 10MΩ
		High	0.0	0.5	1.0	V	
ϕV2	Vertical Clock - Phase 2	Low	-8.5	-8.0	-7.5	V	10nF, 10MΩ
		High	0.0	0.5	1.0	V	
ϕH1	Horizontal Clock - Phase 1	Low	-6.0	-4.0	-2.0	V	100pF, 10MΩ
		High	4.0	+6.0	+8.0	V	
ϕH2	Horizontal Clock - Phase 2	Low	-6.0	-4.0	-2.0	V	100pF, 10MΩ
		High	4.0	+6.0	+8.0	V	
ϕR	Reset Clock	Low	-5.0	-2.0		V	5pF, 10MΩ
		High		+3.0	+5.0	V	

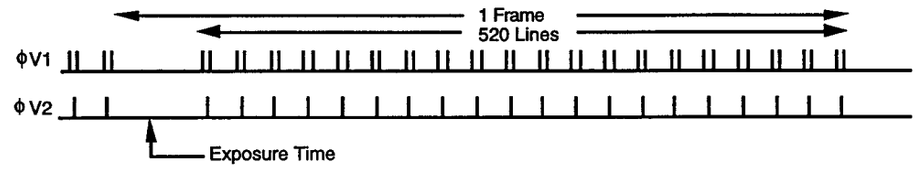
Note: The AC and DC operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages. Pins shown with impedances greater than 1 Mohm are expected resistances. These pins are only verified to 1 Mohm.

Note: This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

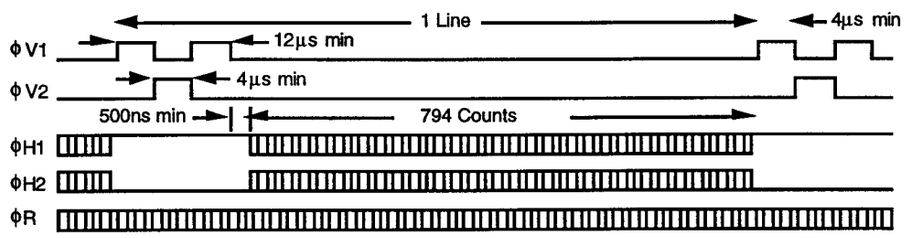
Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

2.5 AC Timing

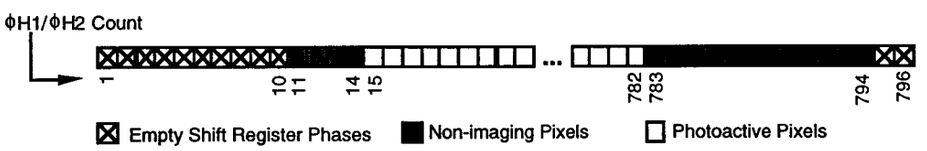
FRAME TIMING



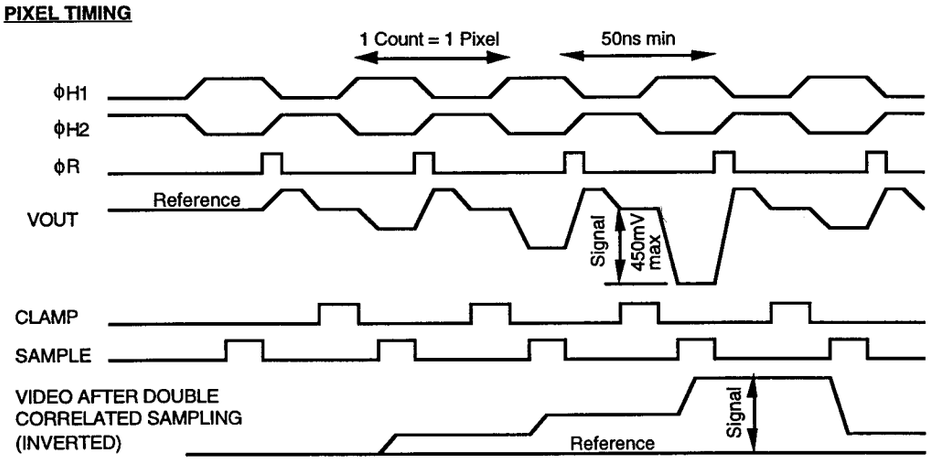
LINE TIMING



LINE CONTENT



PIXEL TIMING



Note: This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult Eastman Kodak in those situations which require special consideration

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

3.1 Image Specifications

All values derived using nominal operating conditions with the recommended timing. Unless otherwise stated, readout time = 50 ms and integration time = 120 ms. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons - to convert to voltage, multiply by the amplifier sensitivity.

Electro-Optical

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	CONDITION
FF	Optical Fill Factor		70		%	
PRNU	Photoresponse Non-uniformity			±5	% rms	Full Array

CCD

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	CONDITION
N_{e^-sat}	Sat. Signal - Vertical CCD Sat. Signal - Horizontal CCD Sat. Signal - Output Node		45 170 340		ke^- ke^- ke^-	
J_d	Dark Current			10 50	pA/cm^2 e^-pixel/sec	Note 1
DCDR	Dark Current Doubling Temp		5	6	^oC	
DSNU	Dark Signal Non-uniformity			4	e^- rms	Note 1
CTE	Charge Transfer Efficiency	.99997	.99999			Note 2
F_H	Horizontal CCD Frequency		10	20	MHz	Note 3
t_{VH}	V-H CCD Transfer Time	4	5		µs	Note 3, 4
L	Image Lag		na			
Bs	Blooming Suppression		300			
S	Smear		na			

Note 1 - For T = 25°C
Note 2 - For 10MHz data rate and T = 40°C
Note 3 - Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance
Note 4 - Time between the rising and falling edges of the vertical clocks

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

Output Amplifier

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	CONDITION
V_{off}	DC Output Level		10		V	
P_d	Power Dissipation		55		mW	
F_{-3dB}	Bandwidth		45		MHz	
A_V	Gain		0.75			
V_{out} / N_{e^-}	Sensitivity (Output Referred)		10		$\mu V/e^-$	
L_i	Non-Linearity		1		%	
C_{load}	Off-chip Load			10	pf	
Z_{out}	Output Impedance		250		Ω	
I_{DD}	VDD supply current		5		mA	
n_{e^-} amp	Read Noise		8	20	e^- rms	Note 1

Note 1 - For data rates greater than 1 MHz

General

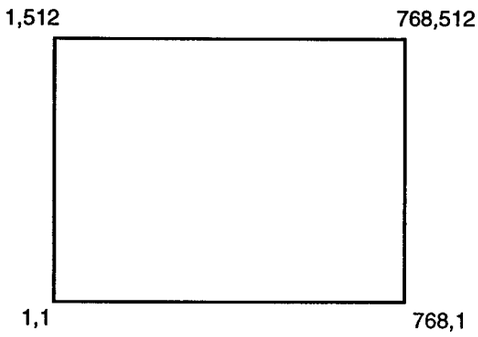
SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	CONDITION
n_{e^-}total	Total Sensor Noise		13	20	e^- rms	Note 1
DR	Dynamic Range		71		db	Note 2
ISO	Equivalent Photographic Speed		TBD			Note 3

Note 1 - Includes amplifier noise, dark pattern noise and dark current shot noise at data rates greater than 1 MHz
Note 2 - Uses 20LOG(N_{e^-} sat / n_{e^-} total) where N_{e^-} sat refers to the vertical CCD saturation signal
Note 3 - Consult Eastman Kodak for use of this parameter

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

3.2 Defect Classification

Class	Point Defects Total	Cluster Defects Total	Column Defects Total
CO	0	0	0
C1	5	0	0
C2	10	4	2



Point Defect	A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation
Cluster Defect	A grouping of not more than 5 adjacent point defects
Column Defect	A grouping of point defects along a single column
Neighboring pixels	The surrounding 100 x 100 pixels or ± 50 columns/rows

Defects are separated by no less than 2 pixels in any one direction

	Test Conditions
Temperature	(T) = 25°C
Integration Time	(t_{int}) = 120msec
Readout Time	($t_{readout}$) = 50msec

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

4.1 Quality Assurance and Reliability

1. Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. The supplier shall be able to demonstrate the existence of these elements.
2. Replacement: All image sensors will be warranted against failures for a period of 1 year from the date of shipment to the customer. This does not include failure due to those mechanical and electrical causes defined as the liability of the customer below.
3. Liability of the Supplier: A reject is defined as an image sensor which does not meet all of the specifications in this document. This will include defects identified up to and including the permanent mounting of the image sensor in the customer's product, not exceeding 1 year from the date of shipment.
4. Liability of the Customer: Damage from mechanical (scratches or breakage), electrical (ESD), or other electrical misuse of the device beyond the stated absolute maximum ratings (section 2.2), which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.
5. Cleanliness: The image sensor shall be free of contamination, scratches, etc. that would cause a visible defect.
6. ESD Precautions: This image sensor should only be handled at static-safe work stations and shipped in a static-safe container.
7. Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied as requested.
8. Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

4.2 Ordering Information

Part Number	Description
KAF-0400C	768 x 512 Full Frame Image Sensor

Address all inquiries and purchase orders to:

Microelectronics Technology Division
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947

4.3 Color Filter Pattern

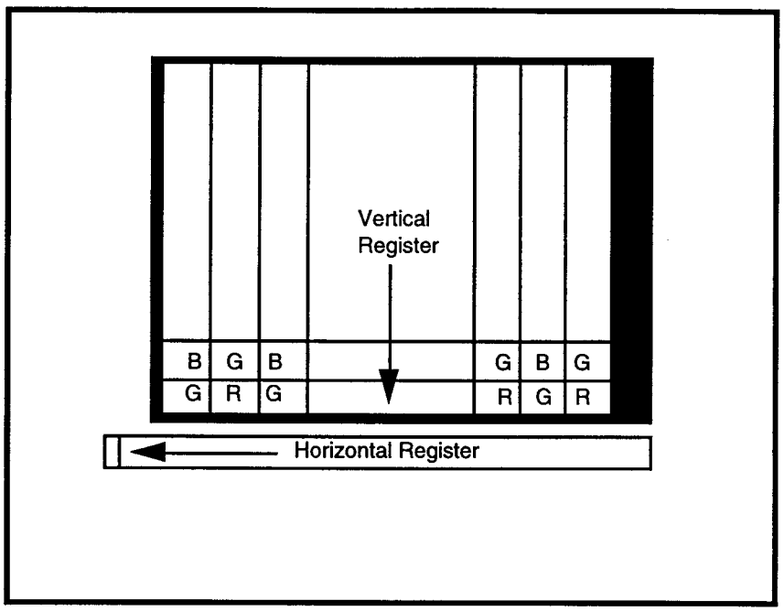


Figure 7 CFA Pattern

Shaded areas represent 4 non-imaging pixels at the beginning and 12 non-imaging pixels at the end of each line. There are 4/4 non-imaging lines at the top/bottom of each frame.

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947

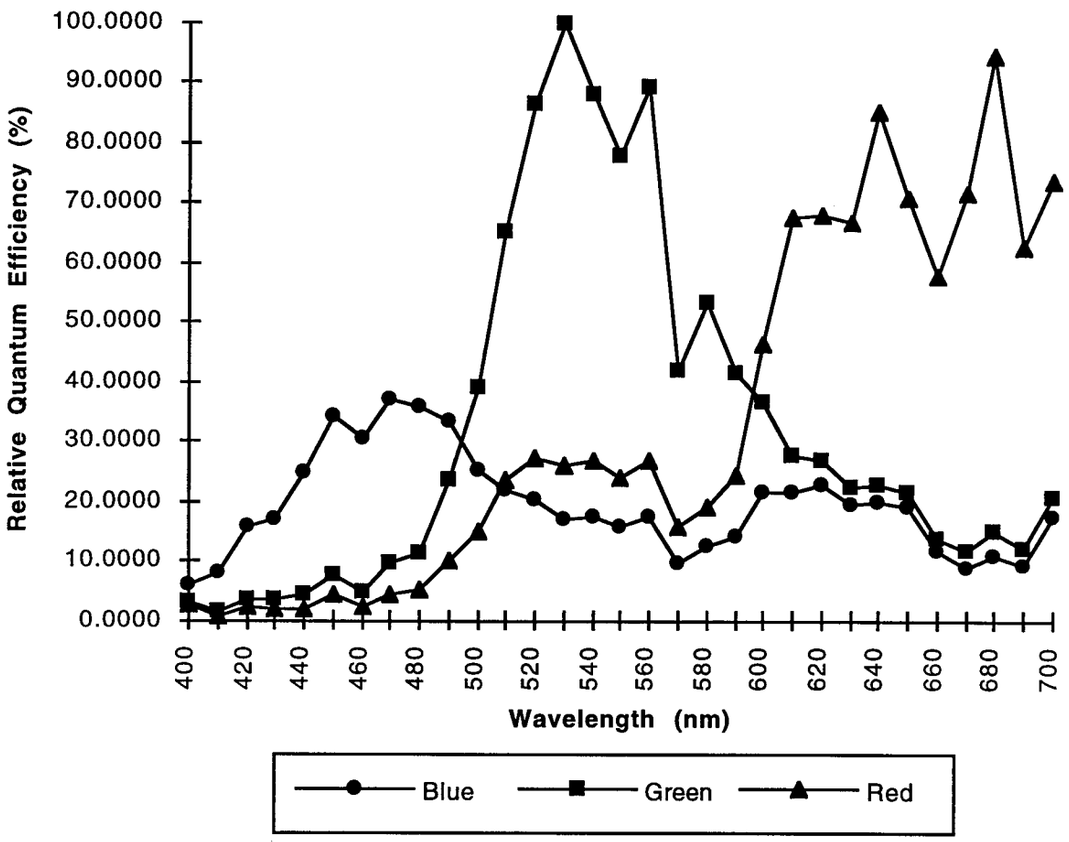


Figure 8 Color Spectral Response

Eastman Kodak Company - Microelectronics Technology Division - Rochester NY 14650-0210
Phone (716)-722-4385 Fax (716)-477-4947